Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-6 (Cancelled)

Claim 7 (Currently Amended): A method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising:

preparing said semiconductor package structured by providing a substrate for mounting said semiconductor element thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on [[the]] an other side of said substrate, and by forming a through hole from the one side to the other side of said substrate, wherein said connecting pattern is exposed at a peripheral area of said through hole;

fixing a surface of said semiconductor element to the one side of said substrate of said semiconductor package such that an electrode of said semiconductor element is within said through hole;

electrically connecting the exposed portion of said connecting pattern and said electrode of said semiconductor element via wires through said through hole; and

sealing said through hole, the exposed portion of said connecting pattern and said wires with resin.

Claim 8 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 7, wherein said connecting pattern is provided continuously in a plurality of stages and the exposed portion of said connecting pattern is provided on a lower stage on the other side of said substrate.

Claim 9 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 7, wherein said through hole comprises a plurality of through holes.

Claim 10 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 7, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package via a tape-bonding material.

Claim 11 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 7, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

Claim 12 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package via a tape-like bonding material.

Claim 13 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 9, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package via a tape-like bonding material.

Claim 14 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 8, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

Claim 15 (Previously Presented): A method of manufacturing a semiconductor device as claimed in claim 9, wherein the surface of said semiconductor element is fixed on the one side of said substrate of said semiconductor package with adhesive.

Claim 16-23 (Canceled)

Claim 24 (Previously Presented): A method of manufacturing a semiconductor device, comprising:

providing a substrate having a first surface and a second surface opposed to the first surface, and further having an elongate opening defined therethrough from the first surface to the second surface;

forming a plurality of connecting patterns on the second surface of said

substrate, each of said connecting patterns having a first end that is exposed at a peripheral area of said elongate opening;

mounting a surface of a semiconductor chip to the first surface of said substrate, wherein a plurality of electrodes are located on the surface of said semiconductor chip and wherein the surface of said semiconductor chip is mounted to the first surface of said substrate such that the electrodes are aligned over said elongate opening of said substrate;

respectively electrically connecting said electrodes to corresponding ones of the first ends of said connecting patterns by a plurality of wires extending from said elongate opening of said substrate to the peripheral area; and

covering said electrodes, said wires, and the first ends of said connecting patterns with a resin.

Claim 25 (Currently Amended): [[The]] A method as claimed in claim 24, wherein said substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein the connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first ends of the connecting patterns are located on said upper plate.

Claim 26 (Previously Presented): A method of manufacturing a semiconductor device, comprising:

providing a substrate having a first surface and a second surface opposed to the first surface, and further having a first elongate opening defined therethrough from the first surface to the second surface and a second elongate opening that is wider than the first opening so that the second elongate opening has a bottom within the substrate;

forming a plurality of connecting patterns on the second surface of said substrate, each of said connecting patterns having a first end that is exposed at the bottom of said second elongate opening;

mounting a surface of a semiconductor chip to the first surface of said substrate, wherein a plurality of electrodes are located on the surface of said semiconductor chip and wherein the surface of said semiconductor chip is mounted to the first surface of said substrate such that each of said electrodes is aligned over said first and second elongate openings of said substrate;

respectively electrically connecting said electrodes to corresponding ones of the first ends of said connecting patterns by a plurality of wires extending from said first elongate opening to said second elongate opening of said substrate; and

covering said electrodes, said wires, and the first ends of said connecting patterns with a resin.

Claim 27 (Previously Presented): A method as claimed in claim 26, wherein said

substrate is provided so as to include an upper plate and a lower plate which define a step configuration in the second surface of said substrate, wherein the upper plate is located between said semiconductor chip and said lower plate, and wherein said connecting patterns are formed so as to extend continuously from said upper plate to said lower plate such that the first ends of said connecting patterns are located on said upper plate.

Claim 28 (Previously Presented): A method of manufacturing a semiconductor device according to claim 7, wherein the resin rises from the other side of said substrate.

Claim 29 (Previously Presented): A method of manufacturing a semiconductor device according to claim 24, wherein the resin rises from the second surface of said substrate.

Claim 30 (Previously Presented): A method of manufacturing a semiconductor device according to claim 26, wherein the resin fully fills said first elongate opening and partially fills said second elongate opening.

Claim 31 (Previously Presented): A method of manufacturing a semiconductor device according to claim 30, wherein a surface of the resin is within said second elongate opening.

Claim 32 (New): A method of manufacturing a semiconductor device as claimed in claim 7, wherein a size of said substrate and a size of said semiconductor element are substantially the same.

Claim 33 (New): A method as claimed in claim 24, wherein a size of said substrate and a size of said semiconductor chip are substantially the same.

Claim 34 (New): A method as claimed in claim 26, wherein a size of said substrate and a size of said semiconductor chip are substantially the same.

Claim 35 (New): A method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising:

preparing said semiconductor package structured by providing a substrate for mounting said semiconductor element thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on an other side of said substrate, and by forming a through hole from the one side to the other side of said substrate, wherein said connecting pattern is exposed at a peripheral area of said through hole;

fixing a surface of said semiconductor element to the one side of said substrate of said semiconductor package such that an electrode of said semiconductor element is within said through hole;

electrically connecting the exposed portion of said connecting pattern and said

electrode of said semiconductor element via wires through said through hole;

sealing said through hole, the exposed portion of said connecting pattern and said wires with resin; and

covering said connecting pattern with an insulating film, wherein a side of said connecting pattern where said wires are connected thereto and parts of said connecting pattern on which external connecting terminals are arranged are not covered by said insulating film,

wherein a size of said substrate and a size of said semiconductor element are substantially the same.